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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/020,967	12/19/2001	Angelo S. Arcaria	87321.1500	1747

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WASHINGTON, DC 20036

EXAMINER

PREVIL, DANIEL

ART UNIT	PAPER NUMBER
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2636

DATE MAILED: 08/15/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/020,967

Applicant(s)

ARCARIA, ANGELO S.

Examiner

Daniel Previl

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 December 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on 19/19/2001 have been accepted for examination purposes only. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heyning et al. (US 4,110,750) in view of Joseph Kelly (US 3,609,020).

Regarding claim 1, Heyning discloses a CPU (microcontroller IC3) and a signal generating circuit (IC2) comprises RC circuitry (fig. 1) having a first capacitor C2 and a second capacitor C3, such that when the first capacitor is switched into the signal generating circuitry by the CPU and the second capacitor is switched into the signal generating circuitry by the CPU (fig. 1).

Heyning discloses the limitations above but fails to explicitly disclose an output signal is produced from the signal generating circuitry that is greater in

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duration than when the first capacitor is switched into the signal generating circuit and the second capacitor is not switched into the signal generating circuitry.

However, Kelly discloses a capacitor 517 having a value of 1000 microfarads having a duration of up to 250 milliseconds (col. 8, lines 62-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Kelly in Heyning. Doing so would produce a sound pleasing to the ear of the listener. Wherein the device is inexpensive, easily programmable of simple design for the sake of the users.

Although, the above combination discloses all the limitations above but fails to explicitly disclose two capacitors produce output signal greater in duration than one capacitor. Since, Kelly discloses a capacitor having a value of 1000 microfarads (col. 8, line 62). So, it would have been obvious to any skill artisan at the time the invention was made to split the capacitor 517 in half wherein each will have 500 microfarads. The split capacitors combined would have a greater output signal in duration than one capacitor in order to produce a sound pleasing to the ear of the listener. Wherein the device is inexpensive, easily programmable of simple design for the sake of the users.

Regarding claim 2, Heyning discloses IC4 outputs a voltage square wave (col. 6, lines 31-47).

Regarding claim 3, Heyning discloses a unity follower circuit that buffers the voltage square wave and generates a buffered voltage (fig. 1).

Regarding claim 4, Heyning discloses an adder circuit that receives the buffered voltage (fig. 1).

Regarding claim 5, Heyning discloses current voltage to the RC circuitry (col. 4, lines 3-19).

Regarding claim 6, Heyning discloses a first voltage divider circuit that establishes a charge voltage on the first capacitor when it is switched into the signal generating circuit and on the second capacitor when it is switched into the signal generating circuitry (fig. 1).

Regarding claim 7, Heyning discloses the charge voltage is input to a first terminal of the adder circuit (fig. 1; col. 6, lines 54-68; col. 7, lines 1-10).

Regarding claim 8, Heyning discloses a diode is in a feedback loop of the adder circuit (fig. 1; col. 5, lines 22-41).

Regarding claim 9, Heyning discloses diode conducts current when the buffered voltage is less than the charge voltage (col. 6, lines 54-68; col. 6, lines 1-10).

Regarding claim 10, Heyning discloses diode does not allow the feedback loop to conduct current when the buffered voltage is greater than the charge voltage (col. 6, lines 54-65).

Regarding claims 11, 14, Heyning discloses a voltage square wave at a node of signal generating circuit (square wave signals at IC4) (fig. 1; col. 6, lines 31-32); generating a charge voltage signal from the charging of at least two capacitors (C5 and C6) (col. 6, lines 31-47); inputting the charge voltage signal to an input of the adder circuit (more than 16 unique inputs for IC3) (fig. 1; col. 4, lines 60-64); outputting to the

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node the charge voltage signal during the time when a voltage of the voltage square wave is lower than the charge voltage (charging rate of a capacitor decay gradually) (col. 7, lines 1-10); outputting the voltage of the voltage square wave when the voltage of the voltage square wave is greater than the charge voltage (when the voltage at output pin is high) (col. 6, lines 54-65).

Heyning discloses the limitations above but fails to explicitly disclose an output signal is produced from the signal generating circuitry that is greater in duration than when the first capacitor is switched into the signal generating circuit and the second capacitor is not switched into the signal generating circuitry.

However, Kelly discloses a capacitor 517 having a value of 1000 microfarads having a duration of up to 250 milliseconds (col. 8, lines 62-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Kelly in Heyning. Doing so would produce a sound pleasing to the ear of the listener. Wherein the device is inexpensive, easily programmable of simple design for the sake of the users.

Although, the above combination discloses all the limitations above but fails to explicitly discloses two capacitors produce output signal greater in duration than one capacitor. Since, Kelly discloses a capacitor having a value of 1000 microfarads (col. 8, line 62). So. It would have been obvious to any skill artisan at the time the invention was made to split the capacitor 517 in half wherein each will have 500 microfarads. The split capacitors combined would have a greater output signal in duration than one capacitor in order to produce a sound pleasing to the ear of the

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listener. Wherein the device is inexpensive, easily programmable of simple design for the sake of the users.

Regarding claim 12 , Heyning discloses the step of generating the voltage square wave from the buffer circuitry (fig. 1).

Regarding claim 13, Heyning discloses the step of utilizing voltage divider circuitry to establish the charge voltage (fig. 1)

Regarding claim 15, Heyning discloses a voltage square wave is a buffer (col. 7, lines 64-66).

Regarding claim 16, Heyning discloses a dc voltage source (inherently included in IC3) (fig. 1).

Regarding claim 17, Heyning discloses the step of inputting the charge voltage signal to an input of the adder circuit is RC circuitry (fig. 1).

Regarding claim 18, Heyning discloses an operational amplifier (col. 6, lines 48-53).

Regarding claims 19-20, Heyning discloses chime device (col. 1, lines 13-14; col. 2, lines 20-21).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

5. Lee et al. (US 6,573,786) discloses an electric devices comprising an audio amplifier and methods for controlling such electronic devices.

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6. Earls et al. (US 4,073,133) discloses an electronic chime and strike system.
7. Durkee (US 4,215,339) discloses an electronic chime.
8. Gaub et al. (US 5,633,625) discloses an electronic chime module and method.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel Previl whose telephone number is 703 305-1028. The examiner can normally be reached on Monday-Thursday. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeff Hofsass can be reached on 703 305-4717. The fax phone numbers for the organization where this application or proceeding is assigned are 703 872-9314 for regular communications and 703 872-9315 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305-4700.

Daniel Previl
Examiner
Art Unit 2636

DP
July 18, 2003


JEFFERY HOFSSASS
SUPERVISORY PATENT EXAMINER
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